

EXPERIMENTAL ANALYSIS OF EXCLUSIVE OR PHASE LOCKED LOOP (PLL)

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ABSTRACT

An experimental analysis of phase locked loop (PLL) circuit has been carried out in order to build and test a simple PLL circuit, determine the lock and capture ranges for a PLL circuit with a traditional XOR phase/frequency comparator, lock and capture ranges for a PLL circuit with sampling type/ frequency comparator and to observe the phase relationship between the input and output waveforms for two common types of phase/frequency detectors. This will enable us ascertain the low power consumption, minimal frequency drift, excellent voltage-controlled oscillator(VCO) frequency linearity and zero voltage offset due to operational amplifier buffering. PLL consists of a phase detector, a loop filter and a voltage-controlled oscillator. The phase detector (PD) and loop combined produces an error signal which amplitude is linearly related to the phase difference of reference and VCO signals. The VCO adjust appropriate to synchronize both signals as desired. PLL in integrated chip 4046BE was studied and the working principles of PLL were verified. Parameters such as capture range and lock range were investigated. The capture range and the lock range of XOR-type PD and the sampling of PD was determined to range between 25 KHz to 40 KHz, 16 KHz to 61 KHz, 26KHz to 75KHz, and 30KHz to 79KHz respectively. The result of this study can be useful for synchronization purposes, provide immunity to substrate noise, power supply or ground voltage fluctuation and other desired effects, in space communication for coherent demodulation and threshold extension, demodulate frequency-modulated signals, synthesize new frequencies which are multiple of a reference frequency etc.

KEYWORDS: Phase Locked Loop, Phase Detector, Variable Controlled Oscillator, Lock Range, Capture Range